HFT Pre-CD2 Deliverables

APV HIP Dead Time

Response to issues raised during

the HFT CD-1 review on Nov. 12, 2009

Dec. 22, 2009

1 Introduction

During the first beam tests of CMS Tracker Outer Barrrel modules[1] an unexpected deadtime was found in the APV25-S1 readout chip[2, 3]. This deadtime is related to very high signals in the silicon sensors and is being caused by inelastic nuclear reactions of the transversing minimum ionizing particles (MIP's) with the bulk silicon of the sensors. These reactions give rise to highly ionizing particles (HIP's) leading to a particular behaviour of all channels in the readout chip. This behaviour was later confirmed with laser tests[4]. Since this effect is unavoidable we will discuss what the expected effect on the performance of the IST at RHICII luminosities will be.

2 Highly ionizing events at RHICII

Simulation studies[5] have shown that essentially each inelastic hadronic interaction in Silicon leads to a HIP event. These interactions lead to recoil Si nuclei or relativily heavy fragments with high ionization densities which could deposit up to a 1000 MIP equivalent but usually maxing out at 100 MIP's.

Since these events are unavoidable a HIP rate estimate has to be made for the IST and the effect on the hit efficiency has to be studied. CMS has done extensive beam test studies of the effect of HIP's on their Silicon strip tracker modules[6]. For both 300 MeV/c and 120 GeV/c pions they found that for 300μm thick silicon sensors the probability was about 10^{-3} per incident pion. Since the most probable pion momentum is roughly the same at RHIC we expect to have the same HIP probability per incident pion.

The expected minimum bias rate for 200 GeV/c Au+Au at RHICII is about 32 kHz while the rates for 500 GeV/c p+p are expected to be 10 MHz. Minimum bias events for 200 GeV/c Au+Au result in an average particle density of about 300 per unit of rapidity at mid-rapidity and is practically flat, as is shown in figure 1. For 500 GeV/c p+p the average particle density is about 3 per unit of rapidity at mid-rapidity and rises when going to higher rapidity, see figure 2. For our calculations we assume it to be flat at a value of 3.5 for $-1 < \eta < +1$.

This leads to fluxes of 10 million and 35 million particles ($\approx$ pions) per unit rapidity per second, for Au+Au and p+p respectivily. This means that if, at mid-rapidity, we cover 1 unit of rapidity with a barrel of 300μm thick silicon then we can expect 1 HIP event per 100μs in that barrel for 200 GeV/c Au+Au and 1 HIP event per 30μs for 500 GeV/c p+p.

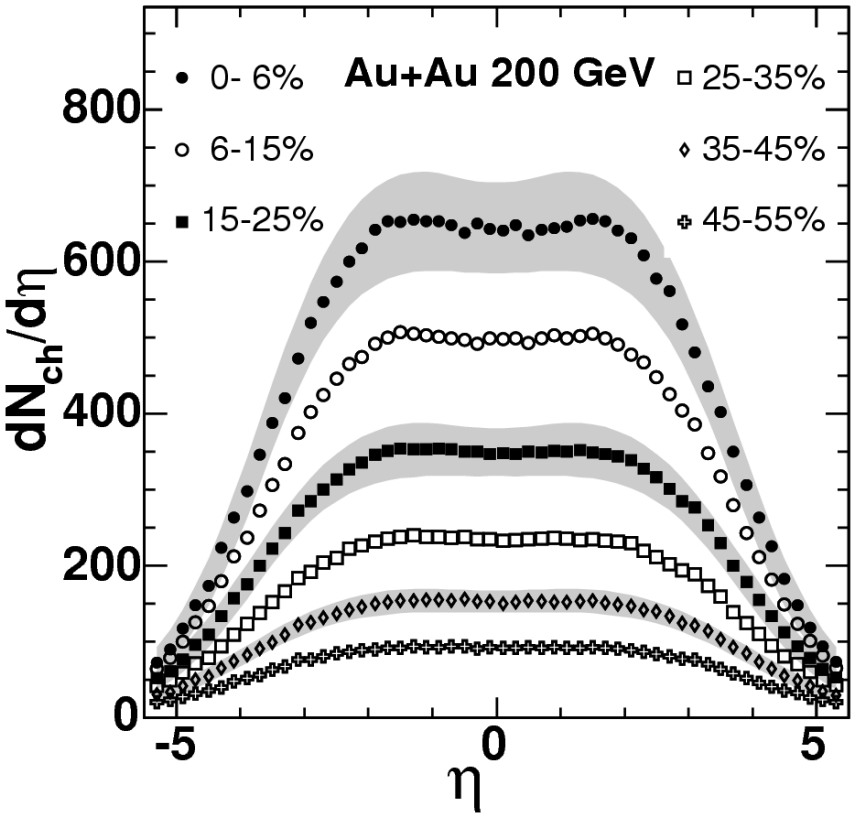

Figure 1: Pseudorapidity density of charged particles emitted in 200 GeV/c Au+Au collisions. Data is given for fractions of the total inelastic cross-section. From [8].

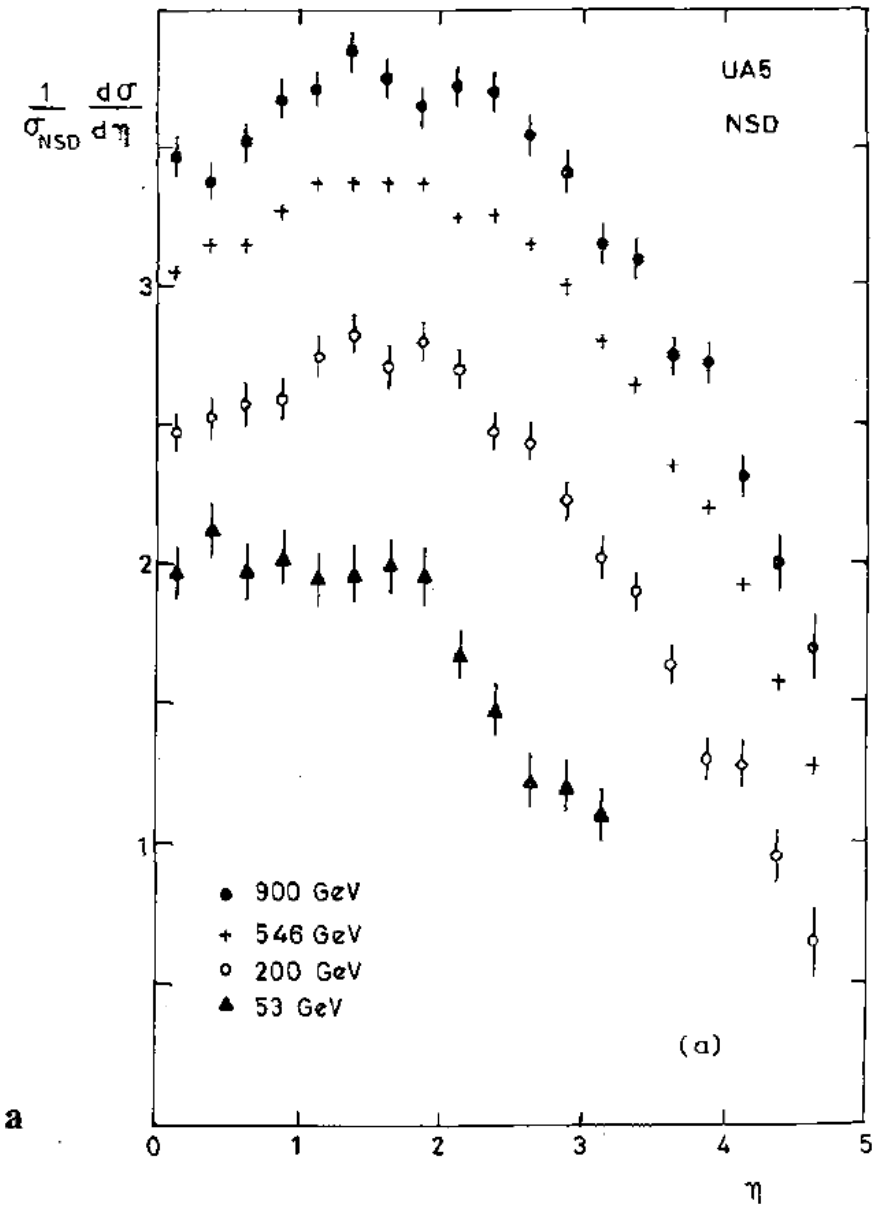

Figure 2: Pseudorapidity density of charged particles emitted in p+p collisions. Data is non single difractive from a range of energies. From [9].

3 APV25-S1 response to HIP events

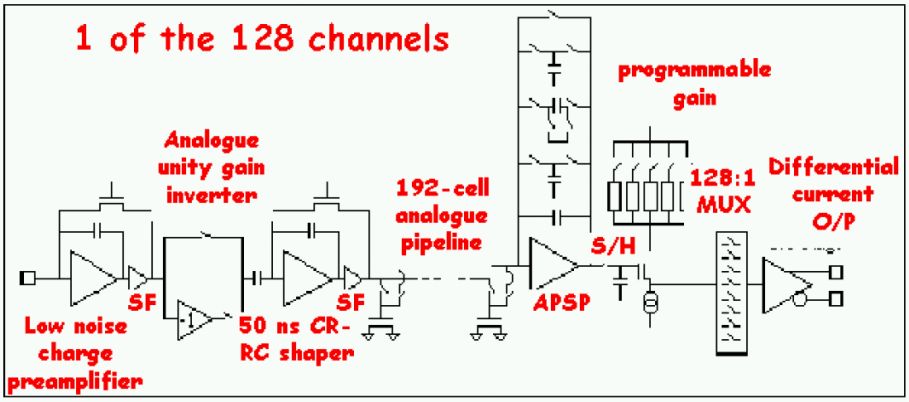

Figure 3: Block diagram of 1 APV25-S1 channel.

Figure 3 shows the block diagram of one channel of the APV25-S1 readout chip that the will use to readout the IST. Unfortunately this chip misbehaves when there is a large (¿ 10 MIP's equivalent) signal on one or more of its inputs. Figure 4 shows 4 APV's of which APV2 gets served a last input signal on one of its inputs (the positive going spike). The result is that for all other channels the baseline gets pulled down. Moreover, the detailed structure of the pulled down channels is unpredictable, making it probably impossible to restore the baseline in software. So, any MIP signals hiding in these channels is most likely lost, leading to hit inefficiencies during the time that the chip needs to restore its baseline. Effectively this leads to a deadtime of the APV after it is being hit by a HIP event.

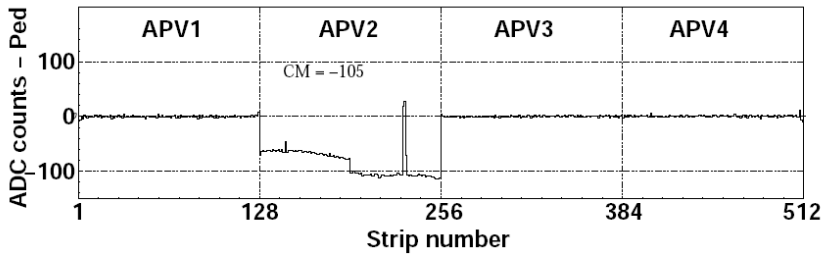

Figure 4: The effect that one large input signal has on a chip, in this case APV2.

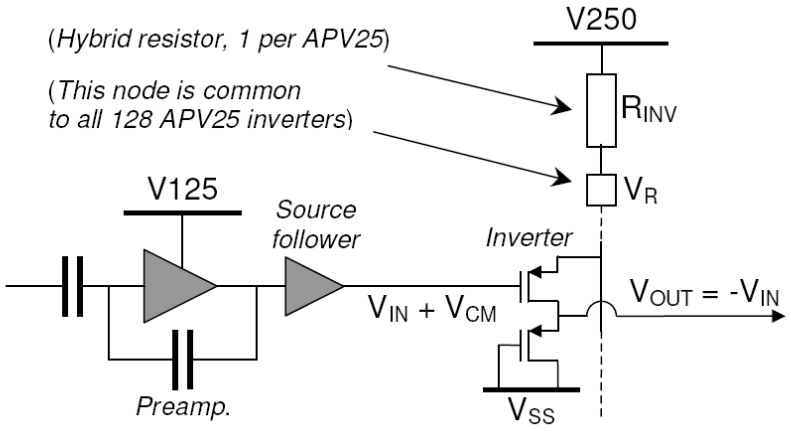

Figure 5: Detail of the inverter stage of the APV25-S1 chip. All inverters are fed by a common rail voltage through one common external resistor.

Figure 5 explains what is happening with the baseline. The inverter stage in each channel makes it possible to use this chips with both negative and positive polarity signals. All inverters are powered by a common rail voltage through a common external resistor. Effectivily this couples all the inverters on a chip which explains why all the baselines get pulled down when there is one big signal introduced in one inverter only. Essentially there will always be a bit of a baseline shift, but for upto a few MIP signals this is hardly noticable. Usually there will be pedestal and common mode noise substraction algorithms active on the data coming off the chip. This software will take care of these small baseline shifts, only for large signals this will become an issue.

What is also an issue is that for large signals the chip will need a certain time to recover from a HIP, it can take upto $rm1\mu s$ before all baselines are properly recovered. During this time it will be difficult to impossible to find MIP's in the channels, the safest is just to throw out the affected chip from the data analysis. Figure 6 shows graphically the baseline restoration time of many APV's after they were faced with a HIP event. The 100Ω is the standard value of the common rail voltage resistor of the invertor circuits. It was found that the baseline restores faster when this resistor value gets lowered, but this decreases the stability of the inverter circuit. We feel that it will be safer to handle the low probability HIP events somehow than to

risk having all readout chips becoming instable.

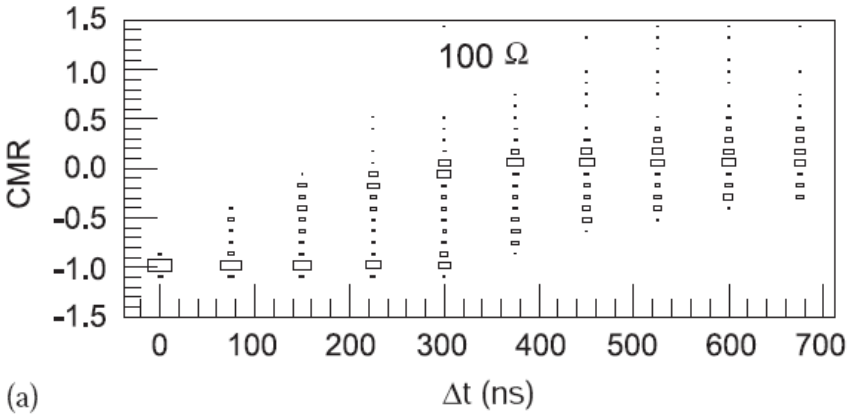

Figure 6: The recovery of the baseline of the APV25-S1 after a HIP event. CMR is a normalized measure of the baseline, with 0 being the standard baseline and -1.0 being the maximum negative baseline. From [7].

4 Effect of HIP events on the performance of the IST

The IST consists roughly of a barrel of 300μm thick silicon sensors at a radius of 14 cm and extending 2.56 units of rapidity symmetrically around mid-rapidity. This silicon is read out by 864 APV25-S1 chips with 128 channels each. Each chip reads out a silicon sensor area of 12.550x38.144 mm^2, figure 7 shows the layout of the IST modules.

According to our calculations in section 2, for 200 GeV Au+Au we can expect 2.56 HIP events per 100μs in the IST. For 500 GeV/c p+p we find 2.56 HIP events per 30μs. This translates to about 1 HIP event per 40μs and 1 HIP event per 12μs, for 200 GeV Au+Au and 500 GeV p+p respectivily.

In section 3 we showed that we can expect a maximum dead time of 1μs for an APV25-S1 readout chip affected by a HIP event. Since the HIP events are mostly characterized by heavier fragments or nuclei with short ranges, we assume that the high energy deposition is contained within the section of the silicon sensor that is read out by 1 APV chip, i.e. only 1 chip is affected by 1 HIP event.

So, for 200 GeV/c Au+Au, on average, we get a collision every 32μs and a HIP event every 40μs. This means that we have to be able to deal with 1 APV25-S1 being dead in every event resulting from a collision. Since the deadtime is 1μs and the collision time is 32μs, there is no 'overflow' to other events. The overall effect for Au+Au is that the IST will operate with 99.9% coverage instead of 100%.

The situation for 500 GeV/c p+p is quite different. We reckon with a collision rate of 100ns and a HIP event every 12μs. The event that 'triggers' the HIP event has only a few particles and the recording of one of them in the IST gets wiped out because of the whole APV25-S1 affected going crazy. The easiest (and probably safest) is just to drop such an event. This means, again on average, 0.8% of the p+p collisions will be useless. Since the deadtime of the affected chip is 1μs there will be an additional 9 collisions which have to deal with 1 chip out of 864 being dead. This means that in those events the IST will operate with 0.1% less coverage.

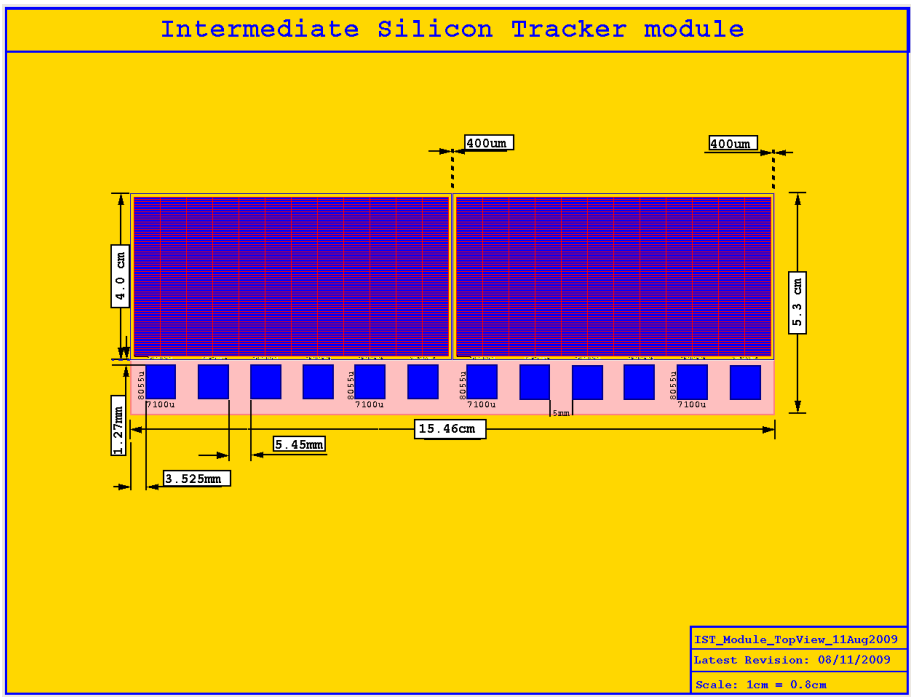

Figure 7: Top view of an IST module, the blue rectangles are the APV25-S1 readout chips. Each chip reads out 2 columns of 64 silicon sensor pads.

5 Conclusion

The Highly Ionizing Particle events observed by CMS during their development test for their silicon tracker will certainly affect the Intermediate Silicon Tracker too. There will be APV25-S1 readout chips that will experience deadtime because of the high signals on their inputs.

However, the effect on the physics operation of the IST should be rather small. For 200 GeV/c Au+Au we expect a loss in coverage of 0.1% for all recorded events because an APV-S1 readout chip is experiencing a 1μs deadtime. For 500 GeV/c p+p we will experience a loss of 0.8% of useful events. On top of that 7.5% of the recorded events will have a loss in coverage of 0.1%.

We don't feel that the described levels of loss in coverage and events warrants further efforts to handle the APV25-S1 deadtime in any other way than just detect HIP events in the recorded data.

References

[1] R. Bainbridge, G. Hall, M. Raymond, The effect of Highly Ionising Events on the APV25 Readout chip, *CMS Note 2002/038*.

[2] L.L. Jones et al., The APV25 deep submicron readout chip for CMS detectors, *CERN/LHCC 1999-033*.

[3] M.J. French et al., *Nucl. Instr. and Meth.* A466 (2001) 359.

[4] J. Bernardini et al., Response of the APV readout chip to laser-simulated, highly ionizing interactions, *CMS Note 2004/022*.

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[6] W. Adam et al., Test-Beam Analysis of the Effect of Highly Ionising Particles on the Silicon Strip Tracker, *CMS Note 2003/025*.

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[8] B.B. Back et al., *Nucl. Phys.* A 757, 28 (2005)

[9] G.J. Alner et al., *Z. Phys.* C33, 1(1986).